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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,424	12/08/2003	Takahiko Murata	82478-3300	2488

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EXAMINER	
BEMBEN, RICHARD M	
ART UNIT	PAPER NUMBER
2622	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,424	MURATA ET AL.	
	Examiner	Art Unit	
	RICHARD M. BEMBEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *4,5,9-11 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species 1 in the reply filed on 28 April 2008 is acknowledged. Species 1 includes claims 1-3, 6-8 and 12-14 (claims 4 & 5 require a fourth voltage pulse, i.e. belong to Species 2).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 6-8 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,181,375 issued to Mitsui et al., hereinafter "Mitsui".

Regarding **claim 1**, Mitsui discloses a charge-coupled device of XY addressing type *(c. 3, l. 15 – c. 4, l. 4; Figures 1 & 2-5, "imaging device 11")*, comprising:

a light-receiving unit that includes an XY matrix of pixel units in each of which photoelectric transfer and charge accumulation are performed *(c. 3, l. 15 – c. 4, l. 4; Figures 1 & 2-5, "imaging device 11" and/or "imaging surface 15")*;

a pulse generating circuit operable to generate two or more types of voltage pulses *(c. 3, ll. 20-24; Figures 1, 2 & 5, "drive circuit 12")*; and

a shift register *(c. 3, ll. 29-34; c. 3, l. 65 – c. 4, l. 19; c. 6, ll. 51-59; Figures 1, 2 & 5, "vertical scanning circuit 16" and/or "horizontal scanning circuit 17")* operable to (a)

start scanning from a first pixel unit that is included in the light-receiving unit, when the two or more types of voltage pulses applied thereto in parallel from the pulse generating circuit are in a first combination, and (b) start scanning from a second pixel unit that is different from the first pixel unit and is included in the light-receiving unit, when the two or more types of the applied voltage pulses are in a second combination that is different from the first combination *(refer to c. 4, l. 20 - c. 5, l. 14 regarding general readout, c. 5. l. . 15 – c. 6, l. 47 and TABLE 1 regarding reading out a selected area, and c. 6, l. 48 - c. 7, l. 11 for a second embodiment of reading out a selected area; also refer to Figures 2, 4A-C & 5)*.

Regarding **claim 2**, refer to the rejection of claim 1 and Mitsui further discloses that the pulse generating circuit generates a first voltage pulse, a second voltage pulse, and a third voltage pulse, each having a voltage level set at HIGH level or LOW level, and applies the first voltage pulse, the second voltage pulse, and the third voltage pulse to the shift register, and the first combination is a combination of the first voltage pulse and the second voltage pulse both being set at HIGH level and the third voltage pulse being set at LOW level at a first time point that is before scanning is started, and the second combination is a combination of the second voltage pulse and the third voltage pulse both being set at HIGH level and the first voltage pulse being set at LOW level at the first time point *(plural pulses generated: refer to Figures 2 & 5-7)*.

Regarding **claim 3**, refer to the rejection of claim 2 and Mitsui further discloses that the shift register includes:

a first pulse output unit operable to output a first selective pulse indicating to select the first pixel unit from the light-receiving unit *(referring to Figures 2 & 5, the pulse output units are the portion of horizontal scanning circuit 17 that output to rows R1-R266)*;

a second pulse output unit operable to output a second selective pulse indicating to select the second pixel unit from the light-receiving unit *(referring to Figures 2 & 5, the pulse output units are the portion of horizontal scanning circuit 17 that output to rows R1-R266)*;

a first scanning start unit operable to output, to the first pulse output unit, a first scanning start pulse indicating to start scanning from the first pixel unit, when the first voltage pulse and the second voltage pulse both being set at HIGH level are applied at the first time point *(referring to Figures 2 & 5, the scanning start units are the portion of horizontal scanning circuit 17 that receive inputs HR, H1, H2, etc.; also refer to Figures 6 & 7 regarding pulses indicating to start scanning; also note that horizontal clock pulses HC1 and HC2 are "selective pulses")*; and

a second scanning start unit operable to output, to the second pulse output unit, a second scanning start pulse indicating to start scanning from the second pixel unit, when the second voltage pulse and the third voltage pulse both being set at HIGH level are applied at the first time point, the first pulse output unit outputs the first selective pulse, when the first scanning start pulse is applied at the first time point and the third

voltage pulse being set at HIGH level is applied at a second time point that follows the first time point, and the second pulse output unit outputs the second selective pulse, when the second scanning start pulse is applied at the first time point and the first voltage pulse being set at HIGH level is applied at the second time point *(referring to Figures 2 & 5, the scanning start units are the portion of horizontal scanning circuit 17 that receive inputs HR, H1, H2, etc.; also refer to Figures 6 & 7 regarding pulses indicating to start scanning; also note that horizontal clock pulses HC1 and HC2 are "selective pulses")*.

Regarding **claim 6**, refer to the rejection of claim 1 and Mitsui further discloses that in the light-receiving unit, a pixel unit belonging to a first column is the first pixel unit, *(c. 3, l. 66 – c. 4, l. 4; c. 5, l. 15 – c. 7, l. 11; TABLE 1; Figures 2 & 4-7)* and a pixel unit belonging to a second column that is different from the first column is the second pixel unit, and the shift register is a horizontal scanning shift register that is placed to extend in an X-axis direction of the light-receiving unit and that scans the light-receiving unit in the X-axis direction *(c. 3, ll. 29-34; c. 3, l. 65 – c. 4, l. 19; c. 6, ll. 51-59; Figures 1, 2 & 5, "horizontal scanning circuit 17")*.

Regarding **claim 7**, refer to the rejection of claim 1 and Mitsui further discloses that the pulse generating circuit generates a first voltage pulse and a second voltage pulse, each having a voltage level set at HIGH level or LOW level, and applies the first voltage pulse and the second voltage pulse to the shift register, and the shift register

starts scanning from the first pixel unit when the first voltage pulse being set at HIGH level and the second voltage pulse being set at LOW level are applied at a first time point that is before scanning is started, and starts scanning from the second pixel unit when the first voltage being set at LOW level and the second voltage pulse being set at HIGH level are applied at the first time point *(c. 5, ll. 22-30; Figures 3A-B and/or c. 6, l. 60 - c. 7, l. 11; Figures 5-7)*.

Regarding **claim 8**, refer to the rejection of claim 7 and Mitsui further discloses that in the light-receiving unit, a pixel unit belonging to a first row is the first pixel unit, and a pixel unit belonging to a second row that is different from the first row is the second pixel unit *(c. 5, ll. 22-30; Figures 3A-B and/or c. 6, l. 60 - c. 7, l. 11; Figures 5-7)*, and the shift register is a vertical scanning shift register that is placed to extend in a Y-axis direction of the light-receiving unit and that scans the light-receiving unit in the Y-axis direction *(c. 3, ll. 29-34; c. 3, l. 65 – c. 4, l. 19; c. 6, ll. 51-59; Figures 1, 2 & 5, "vertical scanning circuit 16")*.

Regarding **claim 12**, Mitsui discloses a charge-coupled device of XY addressing type *(c. 3, l. 15 – c. 4, l. 4; Figures 1 & 2-5, "imaging device 11")*, comprising:

a light-receiving unit that includes an XY matrix of pixel units in each of which photoelectric transfer and charge accumulation are performed *(c. 3, l. 15 – c. 4, l. 4; Figures 1 & 2-5, "imaging device 11" and/or "imaging surface 15")*;

a pulse generating circuit operable to generate two or more types of voltage pulses *(c. 3, ll. 20-24; Figures 1, 2 & 5, "drive circuit 12")*; and

a shift register *(c. 3, ll. 29-34; c. 3, l. 65 – c. 4, l. 19; c. 6, ll. 51-59; Figures 1, 2 & 5, "vertical scanning circuit 16" and/or "horizontal scanning circuit 17")* operable to (a) end scanning at a last pixel unit that is positioned last in a scanning direction in the light-receiving unit, when the two or more types of voltage pulses applied thereto in parallel from the pulse generating circuit are in a combination other than a first combination, and (b) end scanning at a first pixel unit that is different from the last pixel unit and is included in the light-receiving unit, when the two or more types of the applied voltage pulses are in the first combination *(refer to c. 4, l. 20 - c. 5, l. 14 regarding general readout, c. 5. l. . 15 – c. 6, l. 47 and TABLE 1 regarding reading out a selected area, and c. 6, l. 48 - c. 7, l. 11 for a second embodiment of reading out a selected area; also refer to Figures 2, 4A-C & 5)*.

Regarding **claim 13**, refer to the rejection of claim 12 and Mitsui further discloses that the pulse generating circuit generates a first voltage pulse, a second voltage pulse, and a third voltage pulse, each having a voltage level set at HIGH level or LOW level, and applies the first voltage pulse, the second voltage pulse, and the third voltage pulse to the shift register, and the first combination is a combination of the first voltage pulse and the third voltage pulse both being set at HIGH level and the second voltage pulse being set at LOW level at a first time point that is before scanning is ended *(plural pulses generated: refer to Figures 2 & 5-7)*.

Regarding **claim 14**, refer to the rejection of claim 13 and Mitsui further discloses that the shift register includes:

a first pulse output unit operable to output a first selective pulse indicating to select the first pixel unit from the light-receiving unit *(referring to Figures 2 & 5, the pulse output units are the portion of horizontal scanning circuit 17 that output to rows R1-R266)*;

a second pulse output unit operable to output a second selective pulse indicating to select a second pixel unit that is positioned next to the first pixel unit from the light-receiving unit *(referring to Figures 2 & 5, the pulse output units are the portion of horizontal scanning circuit 17 that output to rows R1-R266)*; and

a first scanning end unit operable to output, to the second pulse output unit, a first scanning end pulse indicating to end scanning at the first pixel unit, when the first voltage pulse and the third voltage pulse both being set at HIGH level are applied at the first time point, the first pulse output unit outputs the first selective pulse when the first voltage pulse being set at HIGH level is applied at the first time point, and the second pulse output unit outputs the second selective pulse when the first scanning end pulse is not applied at the first time point, and the second voltage pulse being set at HIGH level is applied at a second time point that follows the first time point, and does not output the second selective pulse when the first scanning end pulse is applied at the first time point even if the second voltage pulse being set at HIGH level is applied at the second time point *(refer to c. 5, l. 15 – c. 7, l. 11, TABLE 1, and Figures 2 & 5, the scanning end units are the portion of horizontal scanning circuit 17 that receive inputs*

HR, H1, H2, etc.; also refer to Figures 6 & 7 regarding pulses indicating to start scanning; also note that horizontal clock pulses HC1 and HC2 are "selective pulses").

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following display the current state of the art for systems and methods that read out a selected area of an image sensor:

US Patent No. 6,765,616 issued to Nakano et al.

US Patent No. 6,700,607 issued to Misawa

US Patent No. 5,196,939 issued to Elabd et al.

US Patent No. 4,910,599 issued to Hashimoto

US Patent No. 4,641,199 issued to Miyagi

US Patent No. 6,839,452 issued to Yang et al.

US Patent No. 6,721,009 issued to Iizuka

US Patent No. 6,597,399 issued to Horii

US Patent No. 6,580,457 issued to Armstrong et al.

US Patent No. 6,400,404 issued to Hirota et al.

US Patent No. 5,363,137 issued to Suga et al.

US Patent No. 5,412,422 issued to Yamada et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD M. BEMBEN whose telephone number is (571)272-7634. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David L. Ometz/
Supervisory Patent Examiner, Art Unit 2622

RMB